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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/870,955	05/30/2001	Klaus-Dieter Hilliges	US20003638	9122

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EXAMINER	
TORRES, JOSEPH D	
ART UNIT	PAPER NUMBER
2133	6

DATE MAILED: 08/28/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/870,955	HILLIGES, KLAUS-DIETER	
	Examiner	Art Unit	
	Joseph D. Torres	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 January 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☒ Claim(s) *15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 May 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *1* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: '890' in Figure 8. A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: '850' on line 23 of page 16 and line 20 of page 18. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

1. Claim 15 is objected to because of the following informalities: 37 CFR 1.75 states that the specification must conclude with a claim particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention or discovery. The preamble of claim 15, "A data media" does not particularly pointing out

the subject matter, which the applicant regards as his invention or discovery and reads as a list of arbitrary means (Note: it is not even clear how the means themselves relate to the data media). The Examiner suggests: A data media for storing computer instructions for automatic test equipment.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-4 and 7-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Cheung, David K. et al. (US 5461310 A, hereafter referred to as Cheung).

35 U.S.C. 102(b) rejection of claim 1.

Cheung teaches automated test equipment ATE (col. 1, lines 13-14, Cheung) comprising: a tester-per-pin architecture having a plurality of individual decentralized per-pin testing units (each of the Pin Slice Circuits in Figure 1 of Cheung is an individual decentralized per-pin testing unit), wherein each per-pin testing unit is adapted for testing a respective pin of a device under test (DUT) by at least one of emitting stimulus response signals to said respective DUT-pin (Driver 26 in Figure 1 of Cheung is a device for emitting stimulus response signals to a respective DUT-pin) and receiving

stimulus response signals from said respective DUT-pin (Comparator 26 in Figure 1 of Cheung is a device for receiving stimulus response signals from a respective DUT-pin), wherein during a testing sequence, the DUT is defined as one or more DUT-cores representing one or more functional units of said DUT and including one or more DUT-pins of said DUT (col. 2, lines 8-15 in Cheung teach that groups of Pin Slice Circuits are used to test different functional components giving an example whereby one 6 pin group is used for testing transistor-transistor logic, TTL, and another grouping of six pins is used for testing Emitter Coupled Logic, ECL, and another grouping comprising the 6 pin group for testing the TTL functional unit and the 6 pin group for testing the ECL functional unit is used to test the combined TTL-ECL functional unit); and means for assigning, during said testing sequence, one or more of said per-pin testing units to one or more ATE-ports (the Abstract in Cheung teaches that participate memory is a means for assigning groupings of Pin Slice Circuits; Note: the pin channels for a grouping comprise an ATE-port for the particular functional unit that is being tested, for example; the 6 pin group for testing the TTL functional unit is an ATE-port, the 6 pin group for testing the ECL functional unit is an ATE-port and the 12 pin group for testing the combined TTL-ECL functional unit is an ATE-port), whereby each ATE-port comprises one or more of said per-pin testing units and represents an independent functional testing unit for testing one or more of said DUT-cores during said testing sequence (col. 2, lines 8-15 in Cheung teach that groups of Pin Slice Circuits are used to test different functional components giving an example whereby one 6 pin group is used for testing transistor-transistor logic, TTL, and another grouping

of six pins is used for testing Emitter Coupled Logic, ECL, and another grouping comprising the 6 pin group for testing the TTL functional unit and the 6 pin group for testing the ECL functional unit is used to test the combined TTL-ECL functional unit).

35 U.S.C. 102(b) rejection of claim 2.

Cheung teaches switching means for switching connections between one or more of said per-pin testing units and one or more of said DUT-pins (the Abstract in Cheung teaches that participate memory is a means for assigning groupings of Pin Slice Circuits, Note: the participate memory is a switching means for switching connections between one or more of said per-pin testing units and one or more of said DUT-pins), and controlling means for controlling the switching of said switching means in accordance with the assigning of said one or more of the per-pin testing units to said one or more ATE-ports during said testing sequence (col. 5, lines 38-42 in Cheung, Note: the group select signal is a controlling means for controlling the switching of said switching means in accordance with the assigning of said one or more of the per-pin testing units to said one or more ATE-ports during said testing sequence).

35 U.S.C. 102(b) rejection of claim 3.

Col. 5, lines 38-42 in Cheung, teach that participate memory is used to program the data pattern.

35 U.S.C. 102(b) rejection of claim 4.

Cheung teaches a means for specifying cycle times of stimulus and response vectors for said at least one ATE-port (col. 15, lines 16-25, Cheung); means for specifying a per-pin timing in terms of sets of available waveforms for each ATE-pin of the one ATE-port (col. 2, lines 26-33, Cheung), whereby each waveform represents a sequence of events of various types occurring at specified instances in time (see Event Sequencer 24 and col.3, lines 27-40 in Cheung); means for specifying a pattern program for the one ATE-port (see Abstract, Cheung); means for specifying a per-pin vector data for each pin of the one ATE-port (col.7, lines 44-46, Cheung); and means for specifying analogue set-up conditions for analogue pins of the one ATE-port (See 12-bit DAC in Figure 6 of Cheung; Note: the Circuit in Figure 6 is the Levels Generator 62 of Figure 1).

35 U.S.C. 102(b) rejection of claims 7 and 8.

Cheung teaches specifying means for specifying an alias mapping between per-pin testing units for a plurality of said ATE-ports (the Abstract in Cheung teaches that participate memory is a means for assigning groupings of Pin Slice Circuits, Note: the participate memory is a specifying means for specifying an alias mapping between per-pin testing units for a plurality of said ATE-ports), for specifying at least one of timing information and a pattern program of one individual ATE-port to apply for the plurality of the ATE-ports for which the alias mapping is defined (col. 2, lines 26-33, Cheung).

35 U.S.C. 102(b) rejection of claim 9.

Cheung teaches means for determining a set of concurrently active ATE-ports during a defined testing sequence (col. 5, lines 31-57, Cheung, Note: each address provides a means for determining a set of concurrently active ATE-ports during a defined testing sequence); means for selecting the ATE-port test conditions for one or more ATE-pins, for selecting an ATE-port timing setup for one or more ATE-pins (col. 2, lines 26-33, Cheung); means for specifying global test conditions to express dependencies between pins of the DUT and the ATE (col. 3, lines 27-40 in Cheung teach a Global Sequencer for specifying global test conditions to express dependencies between pins of the DUT and the ATE); and means for determining a multi-port pattern burst as a sequence of per-ATE-port pattern programs for each ATE-port (col. 3, lines 27-40 in Cheung teach that the Event Sequencer is a means for determining a multi-port pattern burst as a sequence of per-ATE-port pattern programs for each ATE-port).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.

2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims 5, 6 and 10-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cheung, David K. et al. (US 5461310 A, hereafter referred to as Cheung).

35 U.S.C. 103(a) rejection of claims 5 and 6.

Cheung, substantially teaches the claimed invention described in claims 1-4 and 7-9 (as rejected above). In addition, Cheung teaches that a test program is used to operate the ATE in Cheung (col. 3, lines 19-26, Cheung).

However Cheung, does not explicitly teach the various program components to implement each of the ATE testing means taught in the Cheung patent.

The Examiner asserts that it would be obvious to devise the individual aspects of the program means taught in the Cheung patent based on Engineering Design Choices and that one of ordinary skill in the art at the time the invention was made would have been highly motivated to devise the individual aspects of the programming means since the Cheung patent requires a test program for operating the test taught in the Cheung patent.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Cheung by including use of various programming components to implement each of the ATE testing means taught in the Cheung patent. This modification would have been obvious to one of ordinary skill in

the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of various programming components would have provided the opportunity to implement the required test program in the Cheung patent based on obvious Engineering Design Choices.

35 U.S.C. 103(a) rejection of claim 10.

Claim 10 is a methods claim citing substantially all the limitations of apparatus claim 1.

35 U.S.C. 103(a) rejection of claim 11.

Claim 11 is a methods claim citing substantially all the limitations of apparatus claim 3.

35 U.S.C. 103(a) rejection of claim 12.

Claim 12 is a methods claim citing substantially all the limitations of apparatus claim 4.

35 U.S.C. 103(a) rejection of claim 13.

Claim 13 is a methods claim citing substantially all the limitations of apparatus claim 8.

35 U.S.C. 103(a) rejection of claim 14.

Claim 14 is a methods claim citing substantially all the limitations of apparatus claim 9.

35 U.S.C. 103(a) rejection of claim 15.

Claim 15 is a computer related means claim citing substantially all the limitations of

apparatus claim 1.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Turnquist, James Alan (US 6557128 B1) teaches a single ATE system which behaves as multiple logic testers, each operating separately and asynchronously from the other, as well as a conventional single logic tester. Fournel, Jean-Claude et al. (US 5944846 A) teaches equipment for automatically testing electronic components in parallel.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (703) 308-7066. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)-746-7240.

Joseph D. Torres, PhD
Art Unit 2133